EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	"20040015540"	US-PGPUB; USPAT	OR	OFF	2006/05/24 09:54
L2	1	"20030149795"	US-PGPUB; USPAT	OR	OFF	2006/05/24 09:54
L3	14	(san or (storage adj2 network)) and (lun with mask$3) and port and class and ((@ad<"20011005") or (@prad<"20011005") or (@rlad<"20011005"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/05/24 09:54
L4	8	storage with (port and class) near driver and ((@ad<"20011005") or (@prad<"20011005") or (@rlad<"20011005"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/05/24 09:54
L5	7	("5,790,795" "5,802,327" "5,809,224" "5,954,796" "5,960,451" "6,058,489" "6,154,854").pn.	USPAT	OR	OFF	2006/05/24 09:54
L6	40	(san or (storage adj2 network)) and (lun or (logical adj2 number)) and (host adj2 adapter) with driver and ((@ad<"20011005") or (@prad<"20011005") or (@rlad<"20011005"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/05/24 09:54
L7	43	(san or (storage adj2 network)) and (lun with (mask$3 or filter$3)) and access and ((@ad<"20011005") or (@prad<"20011005") or (@rlad<"20011005"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/05/24 09:54
L8	27	(san or (storage adj2 network)) and (lun with (mask$3 or filter$3)) and driver and access and ((@ad<"20011005") or (@prad<"20011005") or (@rlad<"20011005"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/05/24 09:54
L9	1	"6035023".pn.	USPAT	OR	OFF	2006/05/24 09:54
L10	3	(storage adj system adj coupled). ti.	USPAT	OR	OFF	2006/05/24 09:54
L11	27	(san or (storage adj2 network)) and (lun with (mask$3 or filter$3)) and driver and access and ((@ad<"20011005") or (@prad<"20011005") or (@rlad<"20011005"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/05/24 09:54

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L12	7	("5,790,795" "5,802,327" "5,809,224" "5,954,796" "5,960,451" "6,058,489" "6,154,854").pn.	USPAT	OR	OFF	2006/05/24 09:54
L13	2	L12 and mask$3	USPAT	OR	OFF	2006/05/24 09:54
L14	33	(san or (storage adj2 network)) and ((lun or (logical adj2 number)) with (mask$3 or filter$3)) and driver and access$3 and ((@ad<"20011005") or (@prad<"20011005") or (@rlad<"20011005"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/24 09:54
L15	6	L14 not L11	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/24 09:54
L16	2	"6671820".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/24 09:54
L17	4	(719/321,325-326.ccls. or 711/163.ccls.) and ((lun or (logical adj2 number)) with (mask$3 or filter$3)) and driver and access$3 and ((@ad<"20011005") or (@prad<"20011005") or (@rlad<"20011005"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/24 10:01
L20	4	(719/321,325-326.ccls. or 711/100,163.ccls. or 718/104) and ((lun or (logical adj2 number)) with (mask$3 or filter$3)) and driver and access$3 and ((@ad<"20011005") or (@prad<"20011005") or (@rlad<"20011005"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/24 10:06

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1 Associative and Parallel Processors

Kenneth J. Thurber, Leon D. Wald

December 1975 **ACM Computing Surveys (CSUR)**, Volume 7 Issue 4

Publisher: ACM Press

Full text available: pdf(2.62 MB) Additional Information: full citation, references, citings, index terms

2 A Systematic Methodology to Compute the Architectural Vulnerability Factors for a High-Performance Microprocessor

Shubhendu S. Mukherjee, Christopher Weaver, Joel Emer, Steven K. Reinhardt, Todd Austin

December 2003 **Proceedings of the 36th annual IEEE/ACM International Symposium on Microarchitecture**

Publisher: IEEE Computer Society

Full text available: pdf(248.01 KB) Additional Information: full citation, abstract, citings, index terms

Single-event upsets from particle strikes have become akey challenge in microprocessor design. Techniques todeal with these transient faults exist, but come at a cost.Designers clearly require accurate estimates of processorerror rates to make appropriate cost/reliability trade-offs.This paper describes a method for generating theseestimates.A key aspect of this analysis is that some single-bit faults(such as those occurring in the branch predictor) will notproduce an error in a program's output ...

3 An asynchronous matrix-vector multiplier for discrete cosine transform

Kyeounsoo Kim, Peter A. Beerel, Youpyo Hong

August 2000 **Proceedings of the 2000 international symposium on Low power electronics and design**

Publisher: ACM Press

Full text available: pdf(400.48 KB) Additional Information: full citation, abstract, references, index terms

This paper proposes an efficient asynchronous hardwired matrix-vector multiplier for the rwo-dimensional discrete cosine transform and inverse discrete cosine transform (DCT/IDCT). The design achieves low power and high performance by taking advantage of the typically large fraction of zero and small-valued data in DCT and IDCT applications. In particular, it skips multiplication by zero and dynamically activates/deactivates required bit-slices of fine-grain bit-partitioned adders using sim ...

Keyw rds: asynchronous matrix-vector multiplier, discrete cosine transform

4 Parallel-and-vector implementation of the event-driven logic simulation algorithm on the Cray Y-MP supercomputer

A. Bataineh, F. Özgüner
December 1992 **Pr ceedings f the 1992 ACM/IEEE c nference n Supercomputing**
Publisher: IEEE Computer Society Press
Full text available: pdf(926.62 KB) Additional Information: full citation, references, index terms

5 On Application of Output Masking to Undetectable Faults in Synchronous Sequential Circuits with Design-for-Testability Logic
Irith Pomeranz, Sudhakar M. Reddy
November 2003 **Proceedings of the 2003 IEEE/ACM international conference on Computer-aided design**
Publisher: IEEE Computer Society
Full text available: pdf(118.58 KB) Additional Information: full citation, abstract, index terms

Design-for-testability (DFT) for synchronous sequentialcircuits causes redundant faults in the original circuit to bedetectable in the circuit with DFT logic. It has beenargued that such faults should not be detected in order toavoid reducing the yield unnecessarily. One way to dealwith such faults is to mask (or ignore) their fault effectswhen they appear on the circuit outputs, without maskingthe detection of faults that need to be detected. To investigatethe extent to which this can be accom ...

6 WISQ: a restartable architecture using queues
A. R. Pleszkun, J. R. Goodman, W. C. Hsu, R. T. Joersz, G. Bier, P. Woest, P. B. Schechter
June 1987 **Proceedings of the 14th annual international symposium on Computer architecture**
Publisher: ACM Press
Full text available: pdf(1.14 MB) Additional Information: full citation, abstract, references, citings, index terms

In this paper, the WISQ architecture is described. This architecture is designed to achieve high performance by exploiting new compiler technology and using a highly segmented pipeline. By having a highly segmented pipeline, a very-high-speed clock can be used. Since a highly segmented pipeline will require relatively long pipelines, a way must be provided to minimize the effects of pipeline bubbles that are formed due to data and control dependencies. It is also important to provide a way ...

7 VLSI design: A novel architecture for power maskable arithmetic units
L. Benini, A. Macii, E. Macii, E. Omerbegovic, M. Poncino, F. Pro
April 2003 **Proceedings of the 13th ACM Great Lakes symposium on VLSI**
Publisher: ACM Press
Full text available: pdf(166.52 KB) Additional Information: full citation, abstract, references, index terms

Power maskable units have been proposed as a viable solution for preventing side-channel attacks to cryptoprocessors. This paper presents a novel architecture for the implementation of a class of such kinds of units, namely arithmetic components, which find wide usage in cryptographic applications and which are not suitable to traditional masking techniques. Results of extensive exploration and architectural trade-off analysis show the viability of the proposed solution.

Keywords: cryptography, low-power design, security

8 Poster session 2: The design of the fixed point unit for the z990 microprocessor
Fadi Busaba, Timothy Slegel, Steven Carlough, Christopher Krygowski, John G. Rell
April 2004 **Pr ceedings f the 14th ACM Great Lakes symposium on VLSI**
Publisher: ACM Press
Full text available: pdf(171.37 KB) Additional Information: full citation, abstract, references, index terms

The paper presents the design of the Fixed Point Unit (FXU) for the IBM eServer z990 microprocessor (announced in 2Q '03) that runs at 1.2 GHz [2]. The FXU is capable of

executing two Register-Memory instructions including arithmetic instructions and a branch instruction in a single cycle. The FXU executes a total of 369 instructions that operate on variable size operands (1 to 256 bytes). The instruction set include decimal arithmetic with multiplies and divides, binary arithmetic, shifts and r ...

Keyw rds: microprocessor, superscalar FXU

9 General storage protection techniques: Securing distributed storage: challenges, techniques, and systems

Vishal Kher, Yongdae Kim

November 2005 **Proceedings of the 2005 ACM workshop on Storage security and survivability StorageSS '05**

Publisher: ACM Press

Full text available: pdf(294.61 KB) Additional Information: full citation, abstract, references, index terms

The rapid increase of sensitive data and the growing number of government regulations that require longterm data retention and protection have forced enterprises to pay serious attention to storage security. In this paper, we discuss important security issues related to storage and present a comprehensive survey of the security services provided by the existing storage systems. We cover a broad range of the storage security literature, present a critical review of the existing solutions, compare ...

Keywords: authorization, confidentiality, integrity, intrusion detection, privacy

10 Adding a vector unit to a superscalar processor

Francisca Quintana, Jesus Corbal, Roger Espasa, Mateo Valero

May 1999 **Proceedings of the 13th international conference on Supercomputing**

Publisher: ACM Press

Full text available: pdf(1.75 MB) Additional Information: full citation, references, citings, index terms

11 Toward a unified framework for version modeling in engineering databases

Randy H. Katz

December 1990 **ACM Computing Surveys (CSUR)**, Volume 22 Issue 4

Publisher: ACM Press

Full text available: pdf(3.14 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Support for unusual applications such as computer-aided design data has been of increasing interest to database system architects. In this survey, we concentrate on one aspect of such support, namely, version modeling. By this, we mean the concepts suitable for structuring a database of complex engineering artifacts that evolve across multiple representations and over time and the operations through which such artifact descriptions are created and modified. There have been ...

12 Multiscalar processors

Gurindar S. Sohi, Scott E. Breach, T. N. Vijaykumar

May 1995 **ACM SIGARCH Computer Architecture News , Proceedings of the 22nd annual international symposium on Computer architecture ISCA '95**, Volume 23 Issue 2

Publisher: ACM Press

Full text available: pdf(1.44 MB) Additional Information: full citation, abstract, references, citings, index terms

Multiscalar processors use a new, aggressive implementation paradigm for extracting large quantities of instruction level parallelism from ordinary high level language programs. A single program is divided into a collection of tasks by a combination of software and hardware. The tasks are distributed to a number of parallel processing units

which reside within a processor complex. Each of these units fetches and executes instructions belonging to its assigned task. The appearance of a single log ...

13 Multiscalar processors

Gurindar S. Sohi, Scott E. Breach, T. N. Vijaykumar
August 1998 **25 years f the internati nal symp sia n Computer architecture (selected papers)**
Publisher: ACM Press
Full text available: pdf(1.57 MB) Additional Information: full citation, references, citings, index terms

14 Single-pass full-screen hardware accelerated antialiasing

Jin-Aeon Lee, Lee-Sup Kim
August 2000 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS workshop on Graphics hardware**
Publisher: ACM Press
Full text available: pdf(8.82 MB) Additional Information: full citation, references, citings, index terms

Keywords: antialiasing, graphics hardware, parallel computing, rendering hardware

15 Regular circuit fabrics: act two-the industrial perspectives (invited): Design methodology and tools for NEC electronics' structured ASIC ISSP

Takumi Okamoto, Tsutomu Kimoto, Naotaka Maeda
April 2004 **Proceedings of the 2004 international symposium on Physical design**
Publisher: ACM Press
Full text available: pdf(324.94 KB) Additional Information: full citation, abstract, references, index terms

In this paper, we describe a design methodology and tools for NEC Electronics' structured ASIC, *Instant Silicon Solution Platform (ISSP)*, which is being developed to fill the gap between FPGAs and standard cell-based ASICs. The ISSP has a unique regular-fabric architecture designed to achieve both a short time to production and high-performance LSI design. We have developed a special design methodology and tools to fully exploit the capability of this new device. Experimental results for ...

Keywords: ISSP, placement, regular fabric, structured ASIC

16 A parallel bit map processor architecture for DA algorithms

Tom Blank, Mark Stefik, Willem vanCleemput
June 1981 **Proceedings of the 18th conference on Design automation**
Publisher: IEEE Press
Full text available: pdf(748.21 KB) Additional Information: full citation, abstract, references, citings, index terms

Bit maps have been used in many Design Automation (DA) algorithms such as printed circuit board (PCB) layout and integrated circuit (IC) design rule checking (DRC). The attraction of bit maps is that they provide a direct representation of two-dimensional images. The difficulty with large scale use of bit maps (e.g., for DRC on VLSI) is that the large amounts of data can consume impractical amounts of computation on sequential machines. This paper describes a processing architect ...

17 A layout synthesis system for NMOS gate-cells

J. Luhukay, W. J. Kubitz
January 1982 **Pr ceedings f the 19th c nference n Design aut mati n**
Publisher: IEEE Press
Additional Information:

Full text available: pdf(746.30 KB) full citation, abstract, references, citings, index terms

A synthesis system for the automatic layout of NMOS gate cells is described. The cells are based on multigrid cell models and are intended for use as part of a chip synthesis system. An outline of the basic concepts of a CAD procedure for the layout synthesis of such cells is given. The main objective is to generate correct and compact cells with controlled growth in area when subjected to modified speed requirements. Both the layout synthesis procedure itself and algorithms are discussed.< ...

18 A new simple and efficient antialiasing with subpixel masks

Andreas Schilling

July 1991 **ACM SIGGRAPH Computer Graphics , Proceedings of the 18th annual conference on Computer graphics and interactive techniques SIGGRAPH '91**, Volume 25 Issue 4

Publisher: ACM Press

Full text available: pdf(647.92 KB) Additional Information: full citation, abstract, references, citings, index terms

Antialiasing of edges is often performed with the help of subpixel masks that indicate which parts of the pixel are covered by the object that has to be drawn. For this purpose, subpixel masks have to be generated during the scan conversion of an image. This paper introduces a new algorithm for creating subpixel masks that avoids some problems of traditional algorithms, like aliasing of high frequencies or blinking of small moving objects. The new algorithms can be implemented by lookup tables t ...

Keywords: antialiasing, exact area subpixel algorithm

19 Logic fault simulation on a vector hypercube multiprocessor

F. Ozguner, C. Aykanat, O. Khalid

January 1989 **Proceedings of the third conference on Hypercube concurrent computers and applications - Volume 2**

Publisher: ACM Press

Full text available: pdf(847.78 KB) Additional Information: full citation, abstract, references, citings, index terms

Fault simulation is the process of simulating the response of a logic circuit to input patterns in the presence of all possible single faults and is an essential part of test generation for VLSI circuits. Parallelization of the deductive and parallel simulation methods, on a hypercube multiprocessor and vectorization of the parallel simulation method are described. Experimental results are presented.

20 Temperature and power aware architectures: Integrated architectural/physical planning approach for minimization of current surge in high performance clock-gated microprocessors

Yiran Chen, Kaushik Roy, Cheng-Kok Koh

August 2003 **Proceedings of the 2003 international symposium on Low power electronics and design**

Publisher: ACM Press

Full text available: pdf(357.09 KB) Additional Information: full citation, abstract, references, index terms

We propose an integrated architectural/physical planning approach to reduce the power supply noise due to current surge in high performance, general-purpose, clock-gated microprocessors. The proposed approach combines dynamic selection of functional units on-the-fly, dynamic issue width scaling and physical planning with soft module, to balance the current demand across layout. Experimental results show that the proposed approach could reduce the peak noise by 6.54% and consequently, the decoupl ...

Keyw rds: inductive noise, power supply noise

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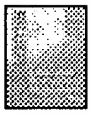
2.	 Book **Solaris™ Guide for Windows NT Administrators** By Tom Bialaski Slots: 1.0 Table of Contents		1. TCP/IP Troubleshooting Tips	Prentice Hall PTR	1!
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